



# SIMCom 5G Series Module RGMII USE NOTE

5G Module

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# 1 Introduction

## 1.1 Document introduction

This document describes design, debug and test notes of RGMII interface, with the help of this document, customers can quickly complete the design and analysis of the problems in the debug and test.

Only SIM8200 and SIM8800 Series modules support RGMII interface, SIM8260X/SIM8360X/SIM8380X Series modules could be extended the RGMII interface through the PCIE Switch chip, such as QPS615.

## 1.2 5G module Models illustrate

The 5G modules include many models, the model definition consists of these parts: module type, application scenario, processor platform, size of package, regional version and package type, for more details please reference figure below.

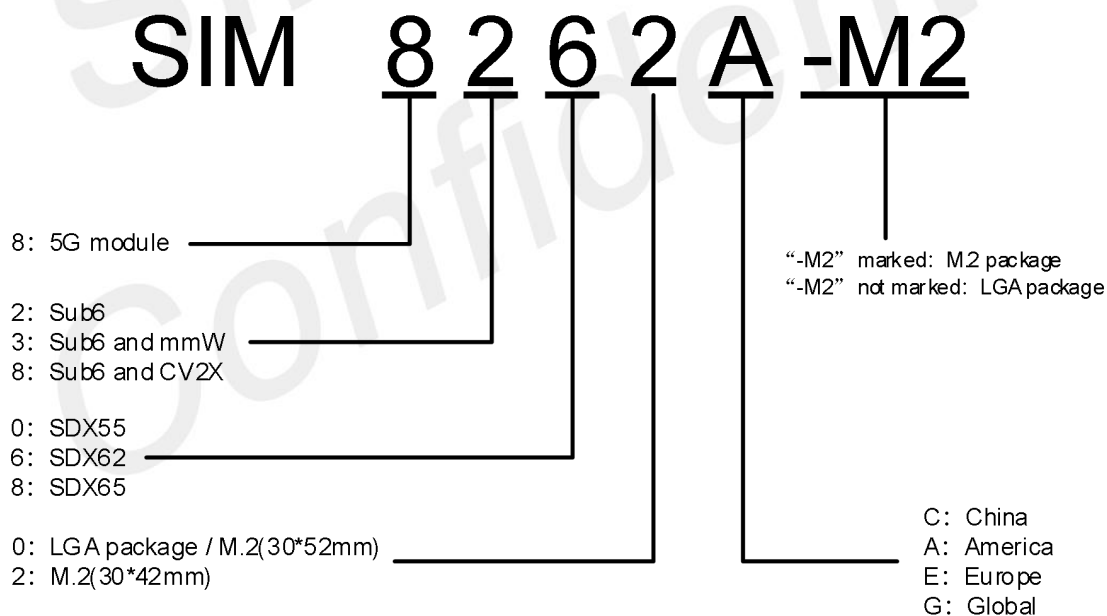


Figure 1: SIMCom 5G Module Model illustrate

## 2 Schematic NOTE

### 2.1 Note the bus signals connect direction and the reserved resistors and capacitors location

The RGMII interfaces TX bus signals of modules include TX\_CLK, TX\_CTL and TX\_0-3 are the data transmit side, they are the data output for 5G modules. The RGMII interfaces RX bus signals of modules include RX\_CLK, RX\_CTL and RX\_0-3 are the data receive side, they are the data input for 5G modules.

Note the TX and RX signals connect direction. The TX signals of modules should connect to RX signals of IC selected by customers, and the RX signals of modules should connect to TX signals of IC selected by customers. Customers should read the datasheet and reference design carefully to make sure the data direction of RGMII signals.

Customer should reserve 22R resistors on RGMII signals, the resistors should place near the data output side as close as possible. TX\_CLK and RX\_CLK signals also should reserve a capacitor in parallel to GND for each, the reserved capacitors should be placed near the data input side as close as possible. The capacitor was used to improve the signals quality of TX\_CLK and RX\_CLK by adjusting the capacitance when the waveform of TX\_CLK or RX\_CLK is not good.

The follow figure shows the module connected to RTL8211F PHY used RGMII interface.

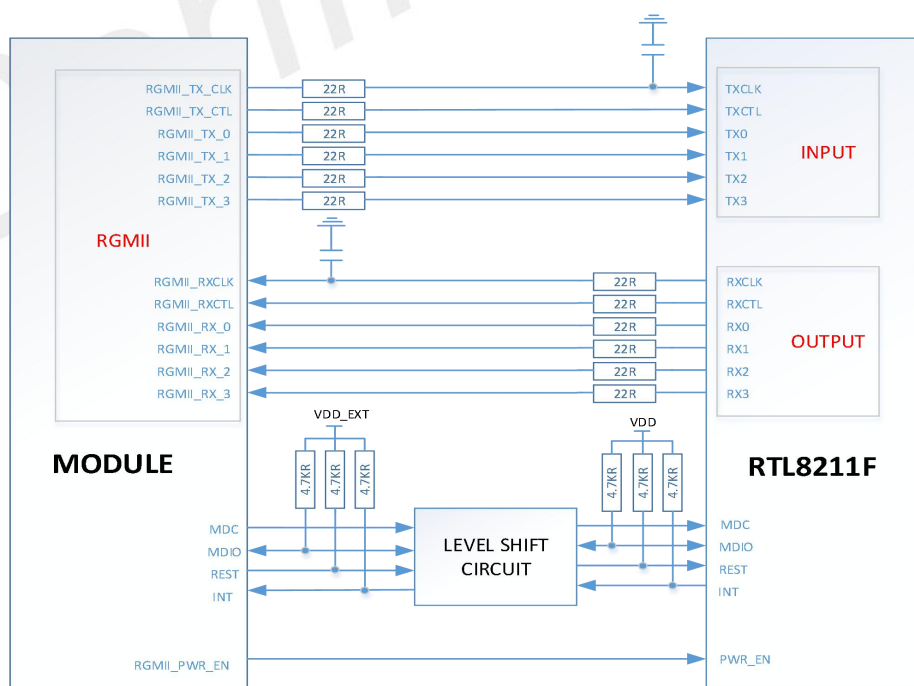


Figure 2: The TX bus and RX bus connect direction of RGMII

## 2.2 Note the RGMII signals voltage domain

In order to ensure the consistency of voltage domain, the modules voltage domain of RGMII signals has fixed to 1.8V, customer should make sure the voltage domain of PHY is set to 1.8V through configuration pin or register.

## 2.3 Note the Level shift chip on the RGMII management signals

The RGMII management signals include MDIO, MDC, RESET and INT.

For LGA modules, if the management signals voltage domain of PHY is 1.8V, customers not need to add level shift chip in design. If the management signals voltage domain of is other voltage domain such as 3.3V, customers need to add level shift chip.

The RGMII signals of MDIO, RESET and INT need to add pull up 4.7KR resistors. It is recommended to reserve pull-up 4.7KR resistors at both side of the level shift chip. The recommended level shift circuit shows as follow figure.

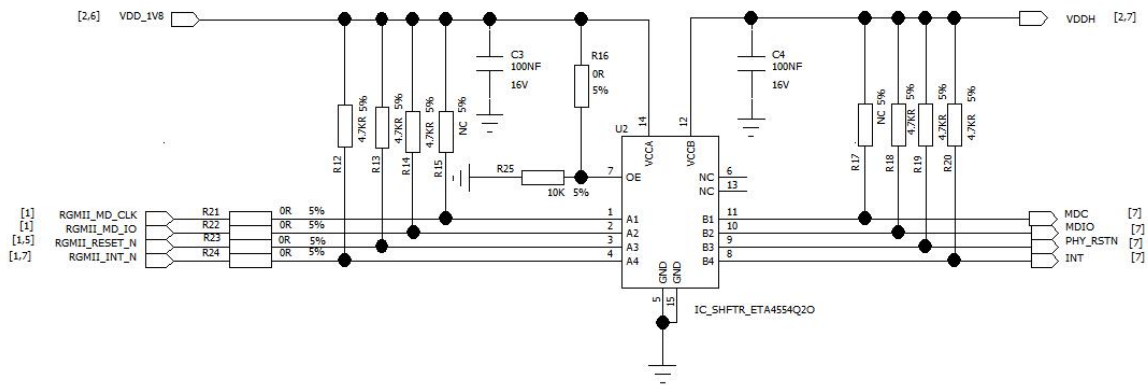


Figure 3: Level shift chip circuit example

The normal waveform before and after level shift chip as shown in the following figure.

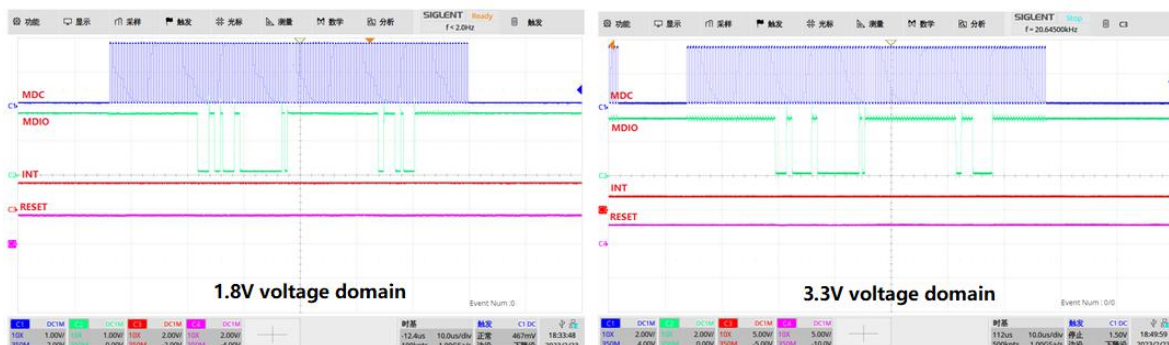


Figure 4: The normal waveform of RGMII management signals (1.8V and 3.3V voltage domain)



Note the OE pin of level shift chip, if customer want use the internal pull-up resistors of level shift chip. The OE pin of level shift chip may high active or low active. When customer selected the level shift chip which the OE pin is high active, if the VCCA is not power on, the OE pin is low, the level shift chip can't be enable and the internal pulled up resistors internal of level shift chip will can't work.

Customer should avoid to select the level shift chip which the OE pin is low active.

The signals of MDC and MDIO are used to configure and manage the PHY. They are used to configure the operating mode and obtain the status information of the PHY chip. Customers can configure the operating mode of the PHY by configuring the register.

Generally, when there is no data transfer, the MDC is low level and the MDIO is high level because the pull up resistor. The follow figure shows the normal waveform of MDC and MDIO.

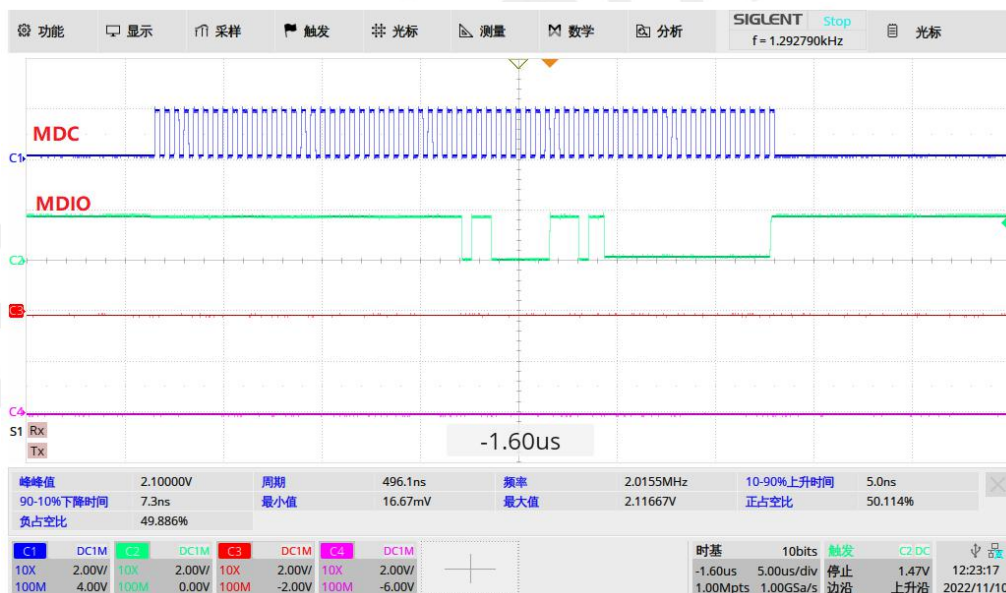


Figure 5: The normal waveform of MDC and MDIO

The RESET signal is used for reset the PHY, active low, the RESET signal has a process of pulling down and then pulling up when initializing the PHY.

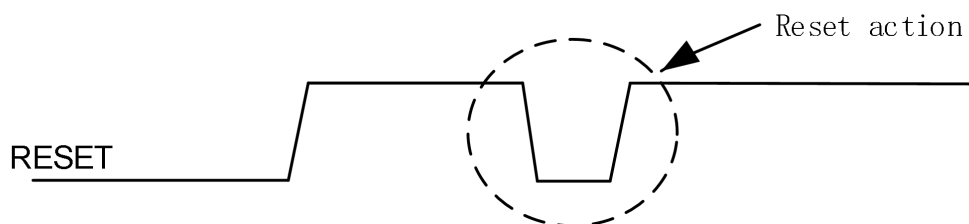


Figure 6: The normal waveform of RESET

The INT signal is an interrupt signal to module, it is an input signal, active low. It is high level when there is no interrupt event occurred. When there is an interrupt event occurred, the INT signal will be pull down and then pull up.

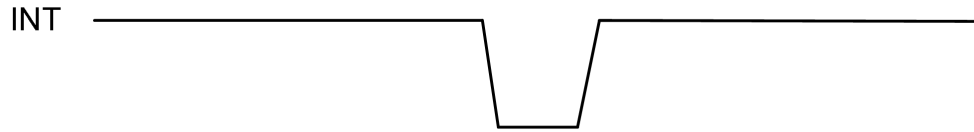


Figure 7: The normal waveform of INT signal when interrupt happened

### 2.3.1 CASE1: The level shift chip model error

In some design, management signals need level shift circuit, but the level shift chip has different types, one of them is designed to capacitive loads, this type level shift chip can't be used to open-drain driver circuit.

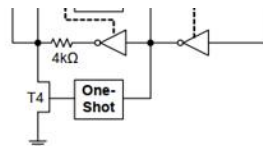


Figure 1. Architecture of SGM4564 I/O Cell

#### Input Driver Requirements

Typical  $I_{IN}$  vs.  $V_{IN}$  characteristics of the SGM4564 are shown in Figure 2. For proper operation, the device driving the data I/Os of the SGM4564 must have drive strength of at least  $\pm 2\text{mA}$ .

#### Pull-Up or Pull-Down Resistors on I/O Lines

The SGM4564 is designed to drive capacitive loads of up to 70pF. The output drivers of the SGM4564 have low DC drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 50kΩ to ensure that they do not contend with the output drivers of the SGM4564.

For the same reason, the SGM4564 should not be used in applications such as I<sup>2</sup>C or 1-wire where an open-drain driver is connected on the bidirectional data I/O.

Figure 8: The level shift chip model error

As follow figure shows, if used the level shift chip which is capacitive loads, the pink waveform is the 1.8v voltage domain, the yellow waveform is the 3.3v voltage domain, the yellow waveform has distorted, and communication between the modules and PHY cannot be completed.

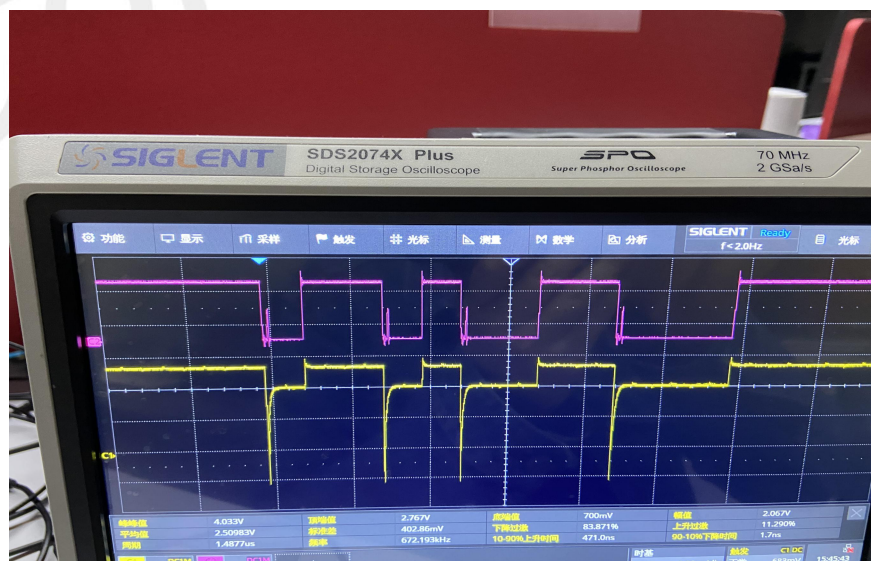


Figure 9: The level shift chip model error caused the waveform distorted

## 3 PCB NOTE

### 3.1 Note the impedance of RGMII signals

The TX bus and RX bus RGMII signals include TX\_CLK, TX\_CTL, TX\_0-3, RX\_CLK, RX\_CTL, RX\_0-3 traces must control 50 ohm differential impedance. According to the stacked structure of the board, customers should calculate the impedance through the Polar Si9000 or other software.

The follow figure shows the impedance of RGMII signals calculation with Si9000.

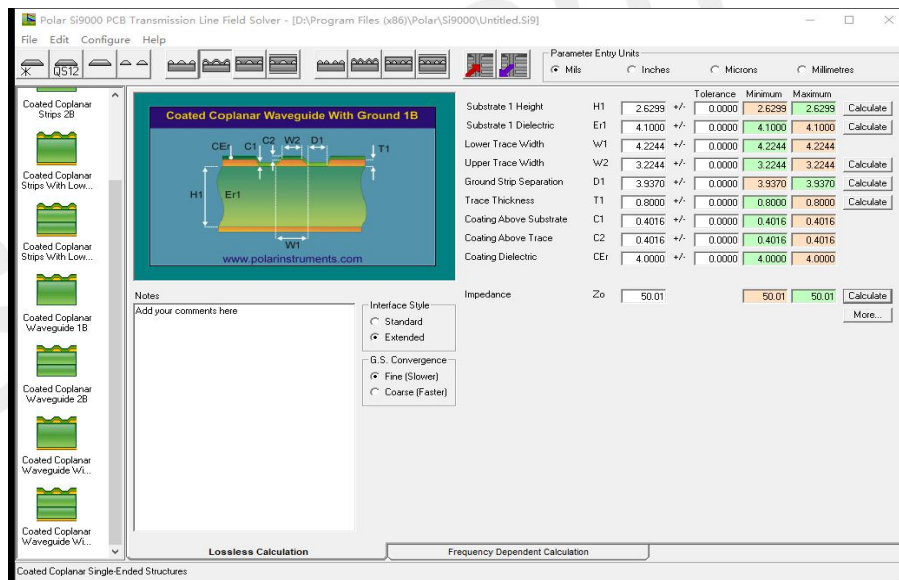


Figure 10: The calculation results of impedance

Impedance mismatch will produce reflections, and the reflection will cause overshoot, ringing, and jitter, and it will cause the slope of rising edge or falling edge to become slowly. The follow figure shows the impedance mismatch caused overshoot and ringing.

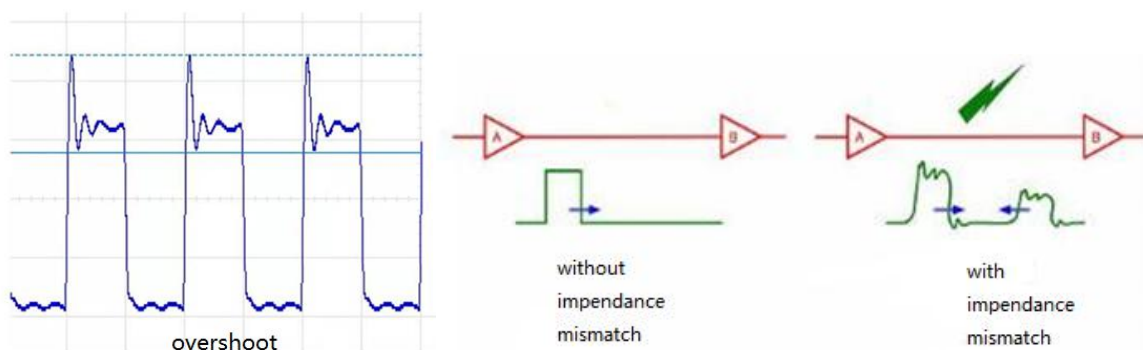


Figure 11: Impedance mismatch caused overshoot and ringing

### 3.2 Note the length of RGMII signals in PCB

For most PHY, the mismatch between the lengths of the TX\_CLK to TX\_CTL, TX\_0-3 and RX\_CLK to RX\_CTL, RX\_0-3 signals should be less than **5mm**. Different PHY has different mismatch length and total length require, please refer to the datasheet and PCB layout guidelines to make sure the mismatch length and total length. Maximum PCB trace length cannot exceed **100mm** out of the module, the shorter trace the better.

The follow figure shows the mismatch length and the total length.

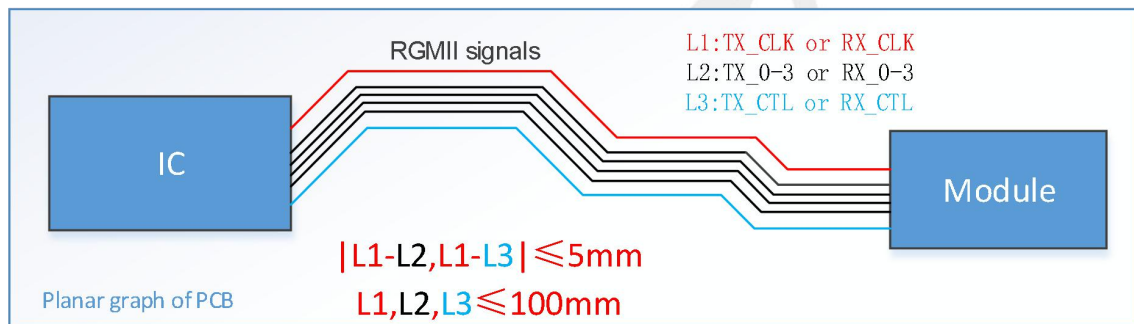


Figure 12: The total length and the mismatch of RGMII

### 3.3 Note the gap of RGMII signals trace

The gap between TX bus and RX bus of RGMII signals trace keeps no less than 2xline width. Gap RX-to-TX keeps no less than 2xline width. Gap to other signals keeps no less than 3xline width.

The follow figure shows the space between TX and RX and between TX and other signals on cutaway view of PCB.

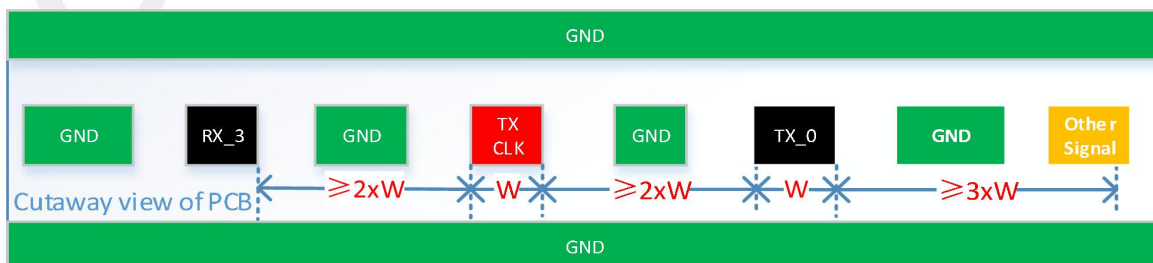


Figure 13: The gap between RGMII signals trace

### 3.3.1 CASE1: The gap of RGMII signals trace is to small

The follow figure shows the gap between TX\_CLK and TX\_CTL, TX\_CLK and TX\_0. The trace width of TX\_CLK is about 0.1mm, the gap between TX\_CLK and TX\_CTL is about 0.08mm, the gap between TX\_CLK and TX\_0 is about 0.07mm. The gap between TX\_CLK and TX\_CTL and the gap between TX\_CLK and TX\_0 are less than 0.2mm (2X TX\_CLK width).

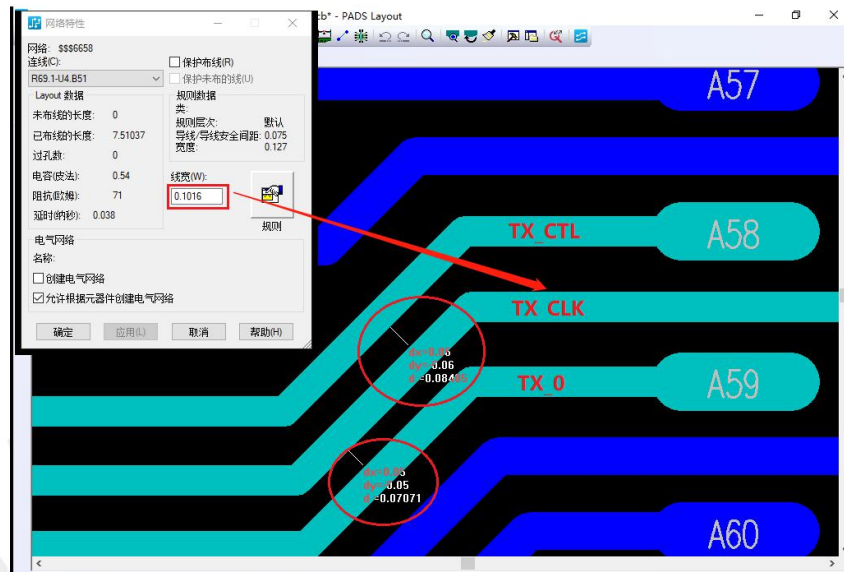


Figure 14: The gap between TX\_CLK and other signals not keep 2xline with

### 3.3.2 CASE2: The TX\_CLK signal is not good caused the PHY can't work

Customer used QCA8337 PHY, but the QCA 8337 cannot communicate with module either in 100M mode and 1000M mode, measure the TX\_CLK waveform of QCA8337 in 100M mode, as follow figure shows the waveform of TX\_CLK is not good.

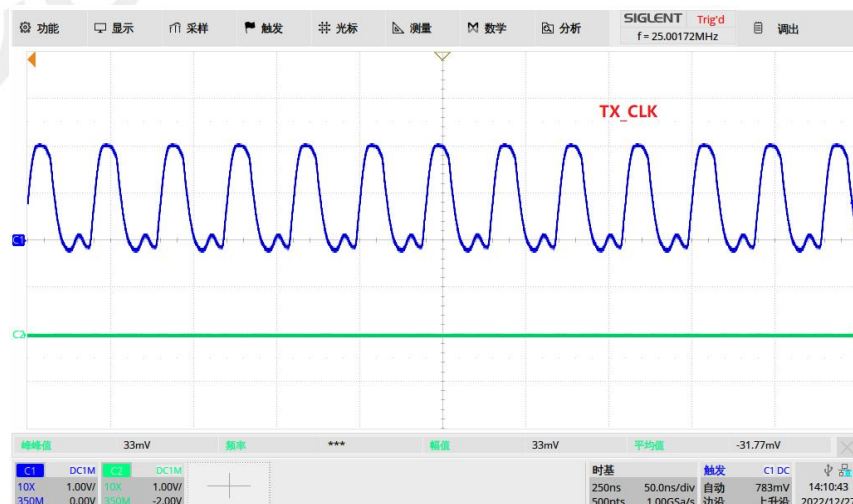


Figure 15: The waveform of TX\_CLK is not good



By adjust the capacitance value between the TX\_CLK and GND such as 15pF, then the waveform of TX\_CLK became normal, and the communication between module and PHY can be completed in 100M mode and 1000M mode.

The follow figure shows the waveform of TX\_CLK after adjust the capacitance value between the TX\_CLK and GND.

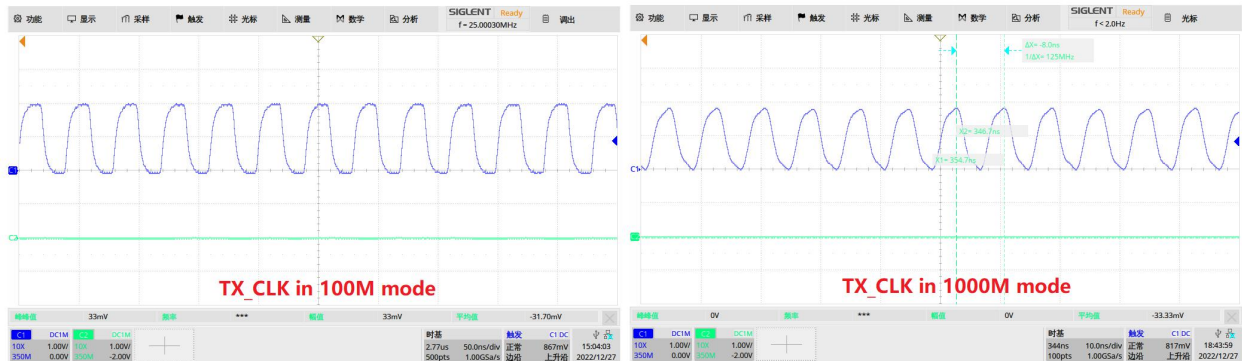


Figure 16: The waveform of TX\_CLK became normal

### 3.4 Note the TX bus and RX bus RGMII signals surround by GND

The RGMII signals should be routed on the inner layer as much as possible, be isolated with GND with solid ground.

The TX\_CLK, RX\_CLK, TX\_CTL and RX\_CTL should surround by GND alone, and the TX\_0-3 bus and RX\_0-3 bus should be surround by GND in a group. The follow figure shows the TX bus signals were surrounded by GND, the RX bus signals are the same as the TX bus signals.

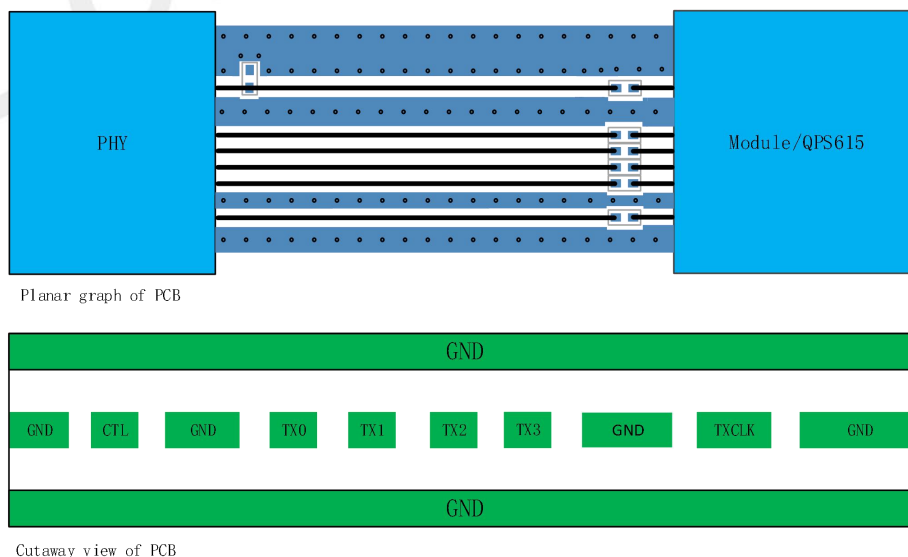


Figure 17: RGMII signals surround by GND

### 3.4.1 CASE1: The RGMII signals trace was surrounded by GND incomplete

The RGMII signals trace was surrounded by GND not enough. As follow figure shows, the RGMII trace has two questions:

- The TX\_CLK and RX\_CLK was not be surround by GND alone.
- The TX\_0-3 bus and RX\_0-3 bus signals was not be surround by GND in a group alone.

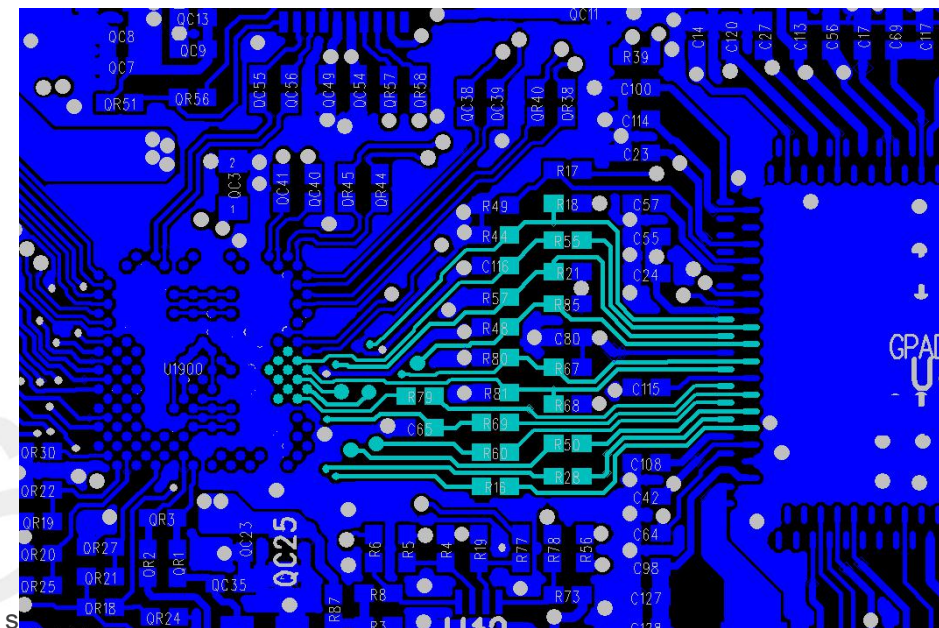


Figure 18: RGMII surrounded by GND incomplete

### 3.5 Note the layout of the RGMII signals avoid forks

The chip customer selected which has configuration function in TX bus or RX bus signals, pay attention to the resistors and capacitors in the TX bus or RX bus trace.

If the resistors and capacitors especially in the TX\_CLK and RX\_CLK were placed to the wrong location, the layout between modules and PHY may caused stub, stubs has a large impact on impedance and can cause signal reflection and overshoot, so customers should usually avoid stubs when designing.

The follow figure shows the RGMII layout comparison of recommend and avoid, customer can layout as the recommend shows.

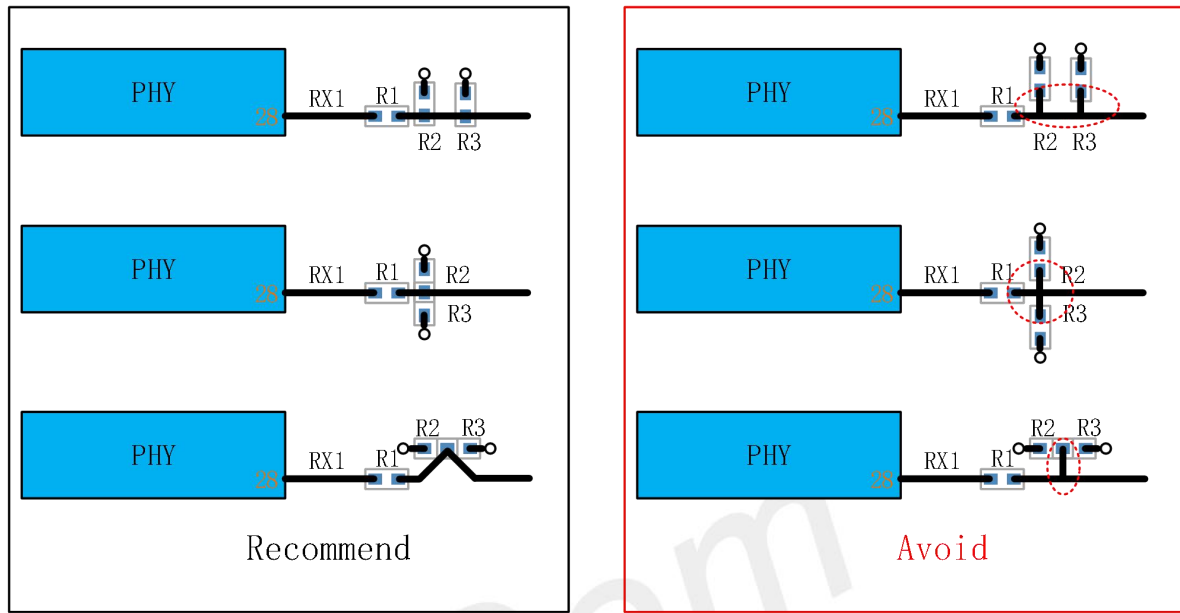


Figure 19: RGMII signals layout avoid forks



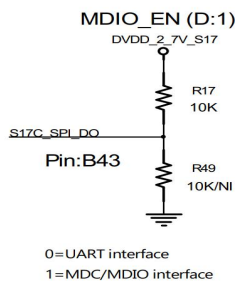
## 4 Configuration NOTE

### 4.1 Note the PHY communication type selection pin

Some PHY has fixed management interface such as MDIO, but some other PHY may have a variety of communication type that can be flexibly selected, such as UART, I<sup>2</sup>C, MDIO or SPI, this types can be selected by configuration pin when the PHY in power-on-strapping status.

When the PHY id can't be recognized, customers should check the communication type selection pin, make sure the pull up or down resistors are right.

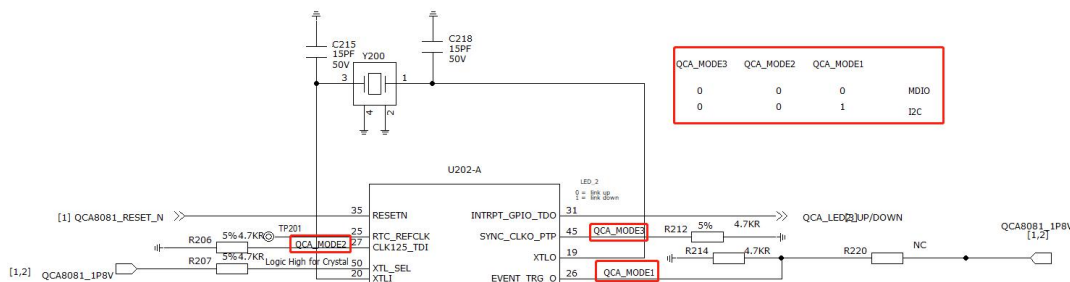
The follow figure shows the QCA8337 PHY chip was set communication type by B43 pin, as the follow schematic shows it was pulled up to 2.7V, so as the follow datasheet shows the communication type is MDC/MDIO.



Pin name	DR-QFN	Power-on configuration	Description
RXD0_0	A55	SPI_EN	0 = No EEPROM connected 1 = EEPROM connected
RXD1_0	B48	SPI_SIZE	0 = 1K 1 = 4K or 2K
RXD2_0	B49	LED_OPEN_EN	0 = Driver 1 = Open drain
RXD3_0	A57	CABLE_DIAG	0 = Disable power-on cable diagnostic 1 = Enable power-on cable diagnostic
SPI_DO	B43	MDIO_EN	0 = UART interface 1 = MDC/MDIO interface

Figure 20: The QCA8337 PHY communication type select

The follow figures show the QEP8121 PHY chip was set communication type by pin 26, 27 and 45, as the follow schematic shows the three pin were pulled down to GND, so as the follow datasheet shows the communication type is MDIO.



Pin number	Power-on strapping name	Description	Default internal weak pull up/down
Management interface			
26	MODE1	MODE[3:1] are latched to select PHY management interface. <ul style="list-style-type: none"> <li>000 = MDIO</li> <li>001 = I<sup>2</sup>C</li> </ul>	Pull down
27	MODE2		Pull down
45	MODE3		Pull down

Figure 21: The QEP8121 PHY communication type select

**Note the communication type between module and PHY is MDIO, other communication type is now support.**

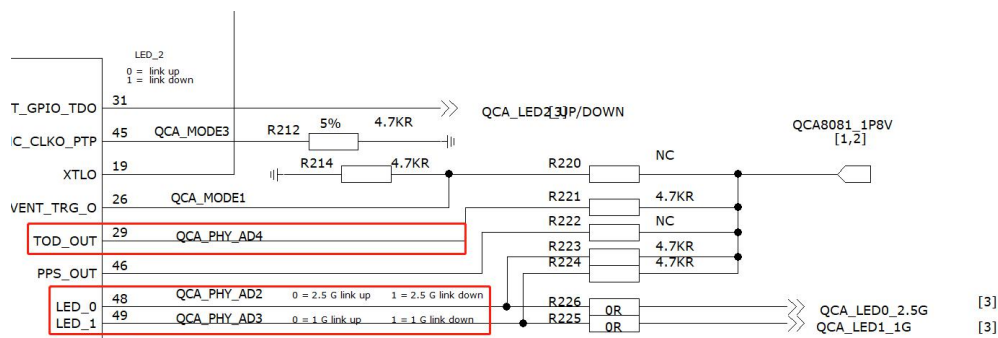
## 4.2 Note the PHY address configuration pin

Some PHY addresses are configured with one or more pins, the PHY address is determined when the PHY in power-on-strapping status.

When the PHY address was be recognized wrong, customers should check the PHY address configuration pin, make sure the pull up or down resistors are on the right location.

Customer can reserve the pull up or down resistors when design the schematic, so that it can be adjusted flexibly according to the debugging.

The follow figures show the QEP8121 PHY address was configured by pin 29, 48 and 49, as the follow schematic shows the three pin were pulled up to 1.8V, as the follow datasheet shows the PHY address is 28.



Pin number	Power-on strapping name	Description	Default internal weak pull up/down
MDIO PHY address			
29	PHYAD4	PHYAD[4:2] are determined by power-on strapping configuration. PHYAD[1:0] are fixed: 00 for PHY core, and 01 for SerDes.	Pull down
49	PHYAD3		Pull down
48	PHYAD2		Pull down

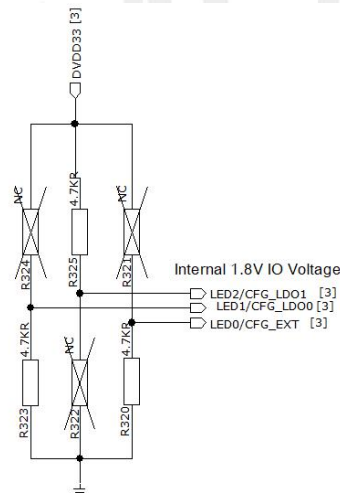
Figure 22: The QEP8121 PHY address configuration

### 4.3 Note the PHY internal power supply

Some PHY chip supply one or more power supply output, this power supply was used for RGMII IO or core supply, customer should note the internal power supply configuration pin, make sure the power supply whether it's internal or external.

Whether used internal or external power supply, customer should make sure the voltage domain of RGMII signals is 1.8V, and should reserve the external DCDC or LDO power supply circuit.

The follow figure shows the power supply selection of RTL8211F PHY, as the follow schematic and datasheet show the LED0/CFG\_EXT pin was pulled up to GND, so the RTL8211F PHY used the internal LDO, the voltage domain of RGMII was set by LED2/CFG\_LDO1 pin and LED1/CFG\_LDO0 pin, LED2/CFG\_LDO1 pin was pulled up to 3.3V and LED1/CFG\_LDO0 pin was pulled down to GND, so the voltage domain of RGMII is 1.8V.



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V(choose)	1'b0	2'b10
Internal 1.5V	1'b0	3'b11

Pin No.	Pin Name	Type	Description
32	CFG_EXT	O/LI/PD	I/O Pad External Power Source Mode Configuration. Pull up to use the external power source for the I/O pad. Pull down to use the integrated LDO to transform the desired voltage for the I/O pad.
33	CFG_LDO0	O/LI/PU	CFG_LDO[1:0]: LDO Output Voltage Selection for the RGMII I/O Pad/ External Power Source Voltage Selection for the RGMII I/O Pad. When pulling down CFG_EXT pin, CFG_LDO[1:0] represent LDO output voltage setting for IO pad: 2'b00: Reserved 2'b01: 2.5V 2'b10: 1.8V 2'b11: 1.5V When pulling up CFG_EXT pin, CFG_LDO[1:0] stand for input voltage selection of the external power for IO pad: 2'b00: 3.3V 2'b01: 2.5V 2'b10: 1.8V 2'b11: 1.5V
34	CFG_LDO1	O/LI/PD	

Figure 23: The RTL8211F PHY internal power supply select

### 4.3.1 CASE1: The ripple of power supply too large caused RGMII can't work normally

Customer has a problem that the downstream rate of RTL8211F is normally, but upstream rate is abnormally, the upstream rate is only 0.02Mbps. When in debugging, customer find the waveform of RX\_CLK is abnormality, the follow figure shows the abnormally upstream rate and waveform of RX\_CLK.

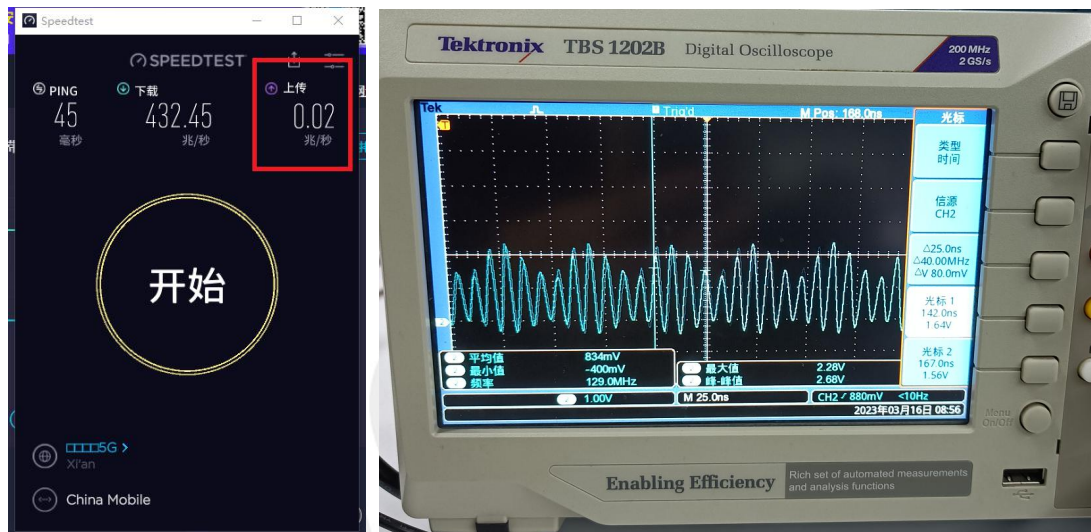


Figure 24: The upstream rate and the waveform of RX\_CLK abnormally

Finally, it was found that the ripple of RGMII IO power supply is too large, it caused the waveform of RX\_CLK and the upstream rate abnormally. As the follow schematic shows, the RGMII voltage domain of RTL8211F was set to use internal LDO, but the resistor R376 was not assembled on the PCB, so the LDO power out pin DVDD\_RG can't be connected to filter capacitors C316 and C317, so the ripple of RGMII IO power supply is too large.

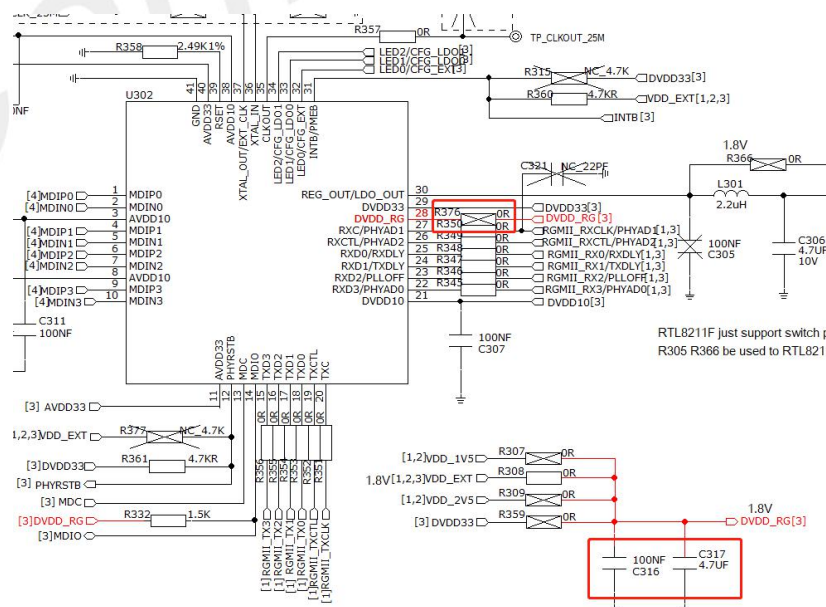


Figure 25: The schematic of RGMII IO power supply



The follow figure shows the ripple of RGMII IO power supply before connect the filter capacitor C316 and C317. The power of RGMII IO is 1.8V, but the ripple is 680mV, it is too large for RTL8211F.



Figure 26: The ripple of RGMII IO power supply before connect the filter capacitor

When the resistor R376 was assembled on the PCB, the filter capacitor C316 and C317 were connected to the RGMII IO power supply, so the ripple of RGMII IO power supply and the waveform of RX\_CLK became normally.

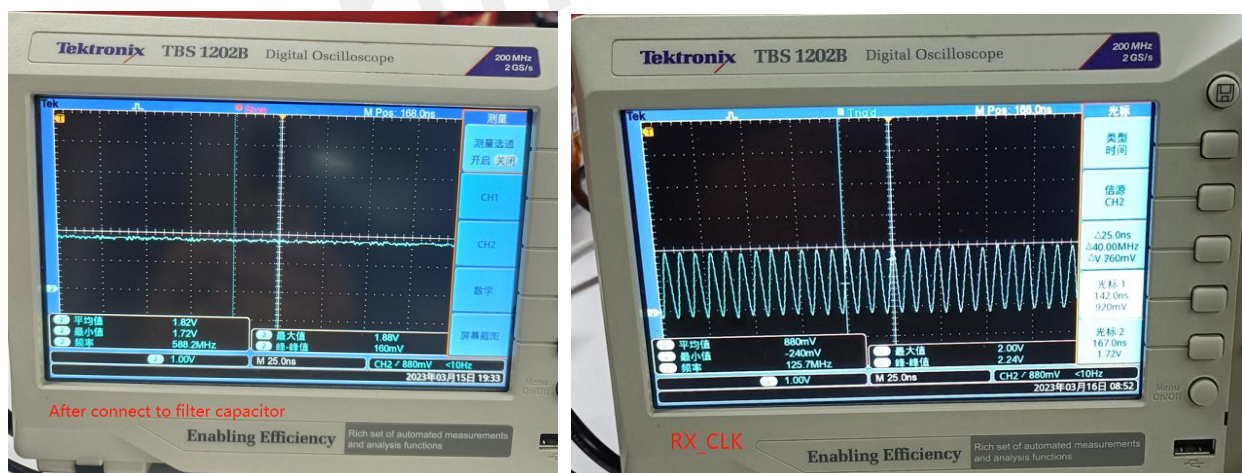


Figure 27: The ripple of RGMII IO power supply and the RX\_CLK became normally

When repeating test the upstream rate, it is normally.

## 4.4 Note the delay configuration pin

In RGMII mode, especially at 1000Mbps, the clock frequency is 125MHz, the data is sampled on the rising and falling edges of the TX\_CLK or RX\_CLK. Ideally, the rising or falling edge of the TX\_CLK or RX\_CLK would be right in the middle of the TX\_0-3 level or RX\_0-3, but there is a delay between the signal line and the clock line.

As the follow figure shows, the rising or falling edge of the TX\_CLK was right in the middle of the TX\_0-3 level at transmitter, but there is a delay between TX\_CLK and TX\_0-3 at receiver.

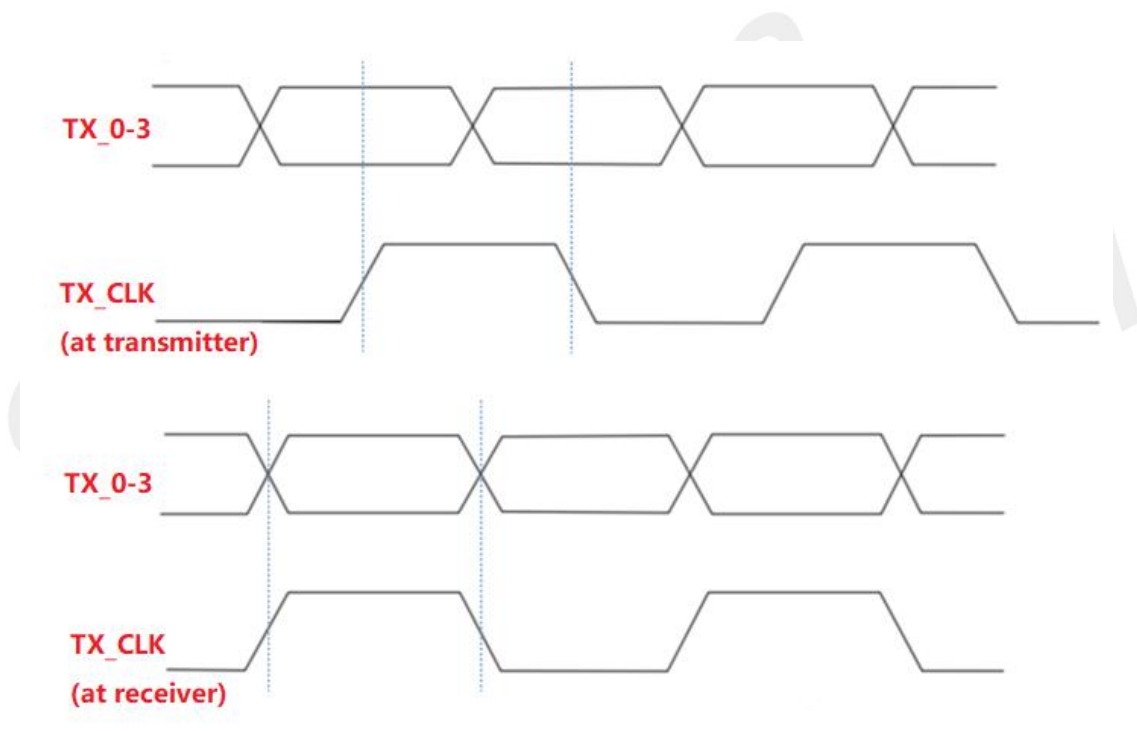


Figure 28: TX\_CLK and TX\_0-3 skew at transmitter and receiver

At receiver, if the rising edge and falling edge of TX\_CLK cannot align with the middle of TX\_0-3, at the time of TX\_0-3 switching, so that the bit of data which was read is not right, and even a bit error will lead to abnormal communication.

Therefore, the receiver end cannot sample stably without additional processing. To solve this problem, a common practice is to add a delay to the clock signal so that its edge is aligned with the stability interval of the data bus. There are three ways to adjust the delay:

1. Delay between TX\_0-3 and TX\_CLK at the sender ;
2. Delay of TX\_0-3 and TX\_CLK caused by PCB trace ;
3. Delay between TX\_0-3 and TX\_CLK at the receiver ;

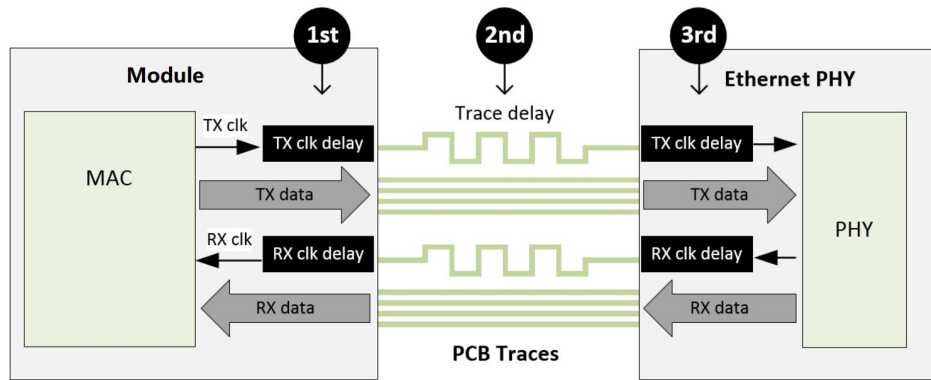


Figure 29: Clock skew stages in the RGMII interface

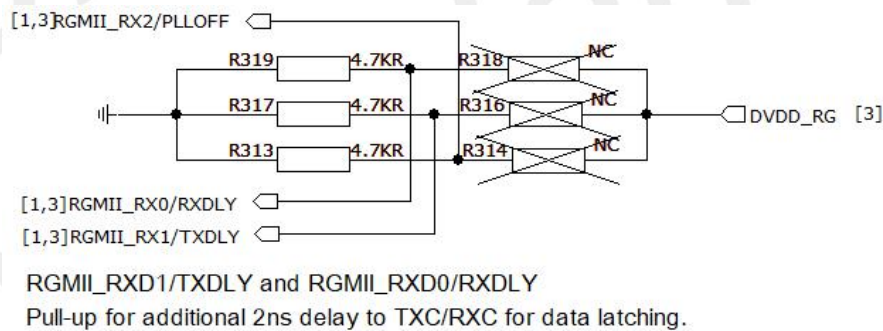
For the first way, the module has fixed the delay of TX\_CLK and RX\_CLK, the delay can't be changed.

For the second way, the PCB traces were equal length, so there is no delay.

For the third way, the TX\_CLK and RX\_CLK could be set by register or configure pins, this is the main way to debug delay.

Customer should control the delay between TX\_CLK and TX\_0-3, so that when TX\_CLK and TX\_0-3 arrive at the receiver, the rising edge and falling edge of TX\_CLK are in the middle of TX\_0-3.

The delay can be set through the register from MDIO interface, or the chip special function pin to configure it in delay mode. The follow figure show the RTL8211F PHY delay configuration from configuration pin and register.



Pin No.	Pin Name	Type	Description
24	TXDLY	O/LI/PD	RGMII Transmit Clock Timing Control. Pull up to enable PHY internal TXC delay.
25	RXDLY	O/LI/PU	RGMII Receiver Clock Timing Control. Pull up to add 2ns delay to RXC for RXD latching.

Figure 30: The RGMII delay configuration from configuration pin

Bits	R/W	Initial value	Mnemonic	Description
25	R/W	0	MAC0_RGMII_TXCLK_DELAY_EN	1 = RGMII interface TXCLK (input from CPU) is delayed. Delay value depends on bits[23:22].
24	R/W	0	Reserved	
23:22	R/W	0	MAC0_RGMII_TXCLK_DELAY_SEL	Control the delay value of RGMII interface TXCLK. 11 = Maximum delay
21:20	R/W	0	MAC0_RGMII_RXCLK_DELAY_SEL	Control the delay value of RGMII interface RXCLK. 11 = Maximum delay

Figure 31: The RGMII delay configuration from register